SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

COMPUTER ORGANIZATION AND ARCHITECTURE

QUESTIONS

ONE MARK:

The output of a NOR gate is HIGH if \_\_\_\_\_\_\_\_.

a.all inputs are HIGH

b.any input is HIGH

c.any input is LOW

d.all inputs are LOW

Base of octal number system is

a.10

b.2

c.8

d.16

Decimal equivalent of hexadecimal no. (44A)16 is :

a.825

b.1098

c.870

d.1100

Binary equivalent of (542)10 is :

a.101010101

b.1110101101

c.101011001

d.1000011110

Convert the binary number 1011011 to hexadecimal.

a.5A

b.5D

c.5B

d.5C

Octal representation of (0101)2 is :

a.5

b.3

c.4

d.6

Cache memory acts between

a.CPU and RAM

b.RAM and ROM

c.CPU and Hard Disk

d.ROM and CPU

Which of the following is lowest in memory hierarchy

a.Cache memory

b.Registers

c.RAM

d.Secondary memory

Which of the following is the correct BCD representation of the decimal number 89?

a.10001001

b.10011001

c.10100001

d.10100101

Which instruction is used for moving the data from accumulator to memory?

a.Move B

b.Store D

c.Load D

d.PUSH A

Which of the following is true about Computer Architecture?

It acts as the interface between hardware and software.

Computer Architecture tells us how exactly all the units in the system are arranged and interconnected.

Computer Architecture is concerned with the structure and behaviour of a computer system as seen by the user.

It involves Physical Components

Which among the following is a type of architecture used in the computers nowadays?

a) Microarchitecture

b) Harvard Architecture

c) Von-Neumann Architecture

d) System Design

In which of the following form the computer stores its data in memory?

Hexadecimal form

Octal form

Binary form

Decimal form

The two’s complement in binary system is useful for expressing

(A) Decimal numbers

(B) Positive numbers

(C) Negative numbers

(D) Binary numbers

The parity bit is added for the purpose of \_\_\_\_\_\_\_\_\_\_\_?

(A) Control key

(B) Error detection

(C) Indexing

(D) Coding

Which of the following is responsible for translating logical addresses to physical addresses?

a) Memory Address Register (MAR)

b) Memory Data Register (MDR)

c) Arithmetic Logic Unit (ALU)

d) Memory Management Unit (MMU)

Find the arithmetic left shift of 1 0 1 0 1

a) 0 1 0 1 0

b) 1 0 1 0 1

c) 0 1 0 1 1

d) 1 0 1 0 0

In 8086 microprocessor , the address bus is bit wide

a) 12 Bit

b) 10 Bit

c) 16 Bit

d) 20 Bit

Use DeMorgan’s theorem to find the complement of A + BC

a) A (B + C)

b) ABC

c) A ( B + C)

d) A ( BC)

Carry lookahead adder logic uses the concept of \_\_\_\_\_\_\_\_\_\_

a) Inverting the inputs

b) Complementing the outputs

c) Carry Propagate and Carry Generate

d) Ripple factor

Which division algorithm is most commonly used for binary division operations?

a) Restoring division

b) Non-restoring division

c) Radix-4 division

d) Booth's division

What are the three components of an IEEE 754 floating-point number representation?

a) Sign exponent and mantissa

b) Sign, integer part and fractional part

c) Mantissa, exponent and bias

d) Sign, exponent and base

Which format is used for double precision floating-point numbers in IEEE 754

a) 64 Bits

b) 32 Bits

c) 16 Bits

d) 128 Bits

Which of the following statements is true for carry-save addition of summands?

a) It can be performed in a single cycle

b) It requires fewer logic gates than carry-propagate addition

c) It always produces the final sum result directly

d) It is only used for fixed-point arithmetic

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Pipelining increases \_\_\_\_\_\_\_\_\_\_\_\_ of the processor

Throughput

Latency

Storage

Predictivity

operand forwarding method does the following to overcome data dependencies

Introduce NULL instructions

Result of the instruction is written to the temporary register

Result of one instruction is directly sent to the next instruction for execution

Blocking the execution of instructions

For a four-stage pipelining, the initial instruction requires \_\_\_\_\_ cycle for execution completion?

2

4

3

1

When the data operands are not available then it is called \_\_\_

Data hazard

Structural hazard

Control hazard

Instruction hazard

Which type of parallelism involves breaking down a program into smaller tasks that can be executed concurrently?

1. Instruction-level parallelism
2. Data-level parallelism
3. Task-level parallelism
4. Pipeline parallelism

Which part of an ARM instruction specifies the operation to be performed?

A. Opcode

B. Data register

C. Memory address

D. Condition code

Which part of an ARM-based system typically handles I/O operations and device communication?

Memory unit

Arithmetic logic unit (ALU)

Input unit

Peripheral interface or controller

What is the primary advantage of the Thumb instruction set in ARM7 architecture?

Greater computational power

Smaller code size

Enhanced multimedia capabilities

Improved memory management

|  |
| --- |
| The stages of 3 stage pipelining are \_\_\_\_.   1. Decode, Fetch, Execute 2. Execute, Fetch, Decode 3. Fetch, Decode, Execute 4. Address generation, Fetch, Execute. |
| R2out , Yin  R3out, Select Y, Add, Zin  Zout, R1in   The above sequence of operations represents   1. R3=R1+R2 2. R1=R2+R3 3. R2=R1+R3 4. R3=R2-R1 |
| The contention for the usage of hardware device is called   1. Data hazard 2. Instruction hazard 3. Structural hazard 4. Stall |
| The conditional branch instruction outcome can be predicted before the execution by using a logic called   1. Branch prediction 2. Delayed branch 3. Structural hazard 4. Static prediction |
| Which addressing mode is capable of working without fetch operation?   1. Register indirect 2. Direct 3. Indexed 4. Immediate |
| In ARM assembly language, what instruction is commonly used for transferring data between memory and registers?   1. ADD 2. MOV 3. SUB 4. CMP |
| What is the purpose of the I/O operations in ARM architecture?   1. To perform arithmetic calculations 2. To manage memory allocation 3. To interact with input and output devices 4. To control processor temperature |
| What type of instruction encoding does ARM7 architecture use?   1. Fixed-length instruction encoding 2. Variable-length instruction encoding 3. CISC (Complex Instruction Set Computer) encoding 4. VLIW (Very Long Instruction Word) encoding |

1. Perform Signed number subtraction using two's complement representation. Subtract: 6 – 3

Subtract: -8 - (-3)

1. Draw the circuit diagram for the following logic expression :AB + BC(B + C).
2. Convert the BCD number 725 to Gray code.
3. Convert decimal (42)10 to Excess-3.
4. Write in detail about the Bus structure in COA.
5. Perform the following conversion
6. One of your tasks is to convert the octal number (176.37)8 to its binary equivalent. Perform the binary to decimal conversion for the given number, (1011100011001.01)₂. Describe the steps you take to convert the binary fractional part to its decimal equivalent, and explain how you combine the integer and fractional parts to obtain the final decimal result. You are a systems hardware engineer working on a project that involves converting numbers between different bases. One of your tasks is to convert the decimal number (7896) 10 to hexadecimal equivalent. iv) Perform BCD addition on the following numbers 652.21 and 345.12
7. i) A student approaches you with a question about subtracting (-19) from (23) using two's complement notation. Explain the step-by-step process of performing this subtraction using the two's complement method. Show the necessary binary conversions, including finding the two's complement of the negative number, and then walk through the binary subtraction and any necessary carry operations. Finally, interpret the binary result back to decimal.

ii) Imagine you're designing a digital circuit that needs to multiply two binary numbers: 01101 and 11010. Perform the binary multiplication step by step, showing all intermediate products and the final result.

iii) Using binary division, compute the quotient and remainder when dividing 011111002 by 00102

Begin by converting the numbers to binary representation and then demonstrate the step-by-step process of binary division. Highlight the key steps involved in each iteration of the division process, including how you determine the next quotient bit and how you adjust the remainder. Conclude by providing the final quotient and remainder in binary and decimal formats.

1. Convert excess-3 1001 to binary. Convert decimal 0 to excess-3 code. Convert binary 1111 to excess-3 code
2. Explain on Input,Output,processing units.
3. 1. Add the following signed binary number a. 111000 + 001101

b. 11001100 + 00010010

12. Utilize  1’s complement and 2’s complement method for the following subtraction (11011)2 – (10011)2

13. A computer has 256 MB of memory. Each word in this computer is eight bytes. How many bits are needed to address any single word in memory?

14. Which part of the functional unit of the computer is known as “Brain”? Justify your answer

15. Imagine you are a computer hardware instructor, and you're leading a workshop on computer architecture for a group of enthusiastic students. To help them grasp the concept of how the processor communicates with memory in a computer system, you decide to provide a hands-on explanation. Could you sketch a diagram that illustrates the connections between the processor and memory components? Additionally, explain how data and instructions flow between these two vital components, highlighting the significance of this interaction in the overall functioning of a computer.

1. State the functions of instructions

ADD R3, - (R4)

ADD R1, (R2)+

1. What is the total memory capacity 8086 processor can address. Write a short note on Memory segmentation used in 8086.
2. In a 4 bit Carry look ahead adder, if the input bits are 1111 and 1101 what is the generate, propagate and carry signal from the third stage.
3. Represent 350.2532 in single precision format.
4. Define addressing modes. With examples explain the following modes.

Register addressing mode

Immediate

Indirect addressing

Relative addressing

1. Write the sequence of instructions that will compute the value of

y = 5x + 6 for a given x using

three-address instructions

two-address instructions

one-address instructions

1. In one rack of library 5 books can be placed, how many racks are needed for 12 books.? Perform the required operation based on the following given algorithm.: Do the following for n times: If the sign of A is 0, shift A and Q left one bit position and subtract M from A, otherwise, shift A and Q left and add M to A. Now, if the sign of A is 0, set q0 to 1, otherwise, set q0 to 0. Step 2: If the sign of A is1, add M to A.
2. Demonstrate the steps involved during Instruction execution and straight-line sequencing with examples
3. i) Find 8 ÷ 7 using Restoring Division (6)
4. ii) Find +13 and -7 using Bit Pair Recoding of Multipliers (6)
5. Design a 4-stage instruction pipeline for 3 instructions I1,I2,I3 to be executed. Consider that there are no dependency between the instructions.
6. Discuss the five step Sequential execution with example
7. Discuss the concepts involved in ILP and how many unit of time to complete the operations

x= a+b

y=c-d

z=x \* y

1. Navin and Vincy are having equal number of apples and it’s count are stored in the register R1 and R2 respectively. Navin collected Vincy’s apple and store the entire set of apples with him and update its count in R1. Write the complete set of control sequences for the above operation.
2. Illustrate the scenario where instructional hazard occurs and provide the solution for handling the stall created by conditional branch instruction.
3. Explain the various types of Parallelism.
4. With the evolution of computing, multi-core processors have become a standard in modern computer architectures.

Define and differentiate between a processor and CPU cores. (4 marks)

Discuss the advantages and potential challenges of multi-core processors compared to single-core processors. (6 marks)

1. What is the sequence of operations for the instruction?

Move R2,(R1)?

1. Differentiate the Memory mapped I/O and I/O mapped I/O
2. Write the sequence of control steps required for single bus structure for following instructions.

Add the immediate number NUM to register R1.

Add the contents of memory location NUM to register R1

1. Draw and explain the structure of ARM registers and processor modes
2. Discuss in details about Restoring Division and Non-Restoring Division with

suitable example and how it is different from each other?

1. 14. Design the 4-bit ripple carry adder and explain it with an example, and discuss its

applications.

1. Explain MISD and MIMD with suitable example.
2. Explain the concept of Flynn’s classification with neat diagram.
3. Explain in detail about Thumb instruction set.
4. List out the Instruction encoding format with example.
5. What is Memory? List out the differences between load and store instruction. Explain along with example instructions.
6. Discuss the challenges in parallel processing with necessary examples.
7. Explain Flynn’s classification of parallel processing with necessary diagrams.
8. What are the various logical operations and explain the instructions supporting the
9. logical operations.
10. Discuss in details about I/O operations along with suitable example.
11. Describe and details about ARM Processor.
12. Briefly explain with neat diagram about ARM 5 Processor.
13. Briefly explain with neat diagram about ARM 7 Processor.

**Q1.**There is an instruction pipeline with four stages. The stage delays for each stage is 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. Consider the delay of an inter-stage

register in the  pipeline is 1 nsec. Find the approximate speedup of the pipeline in the steady state under ideal conditions as compare to to the corresponding non-pipelined implementation?

(a) 4.0

(b) 2.5

(c) 1.1

(d) 3.0

**Answer :** Correct option is (b).

**Explanation-**

When N instruction will be execute in non pipeline manner the time taken will be equal be (5 + 6 + 11 + 8) \* N = 30N

Now we will calculate the clock period for pipelined implementation and it will be equal to  max{5,6,11,8} + 1 = 12.

Time taken in execution of N instruction through pipelined will be equal to  12N (approx.)

So Speedup = 30N / 12N = 2.5

 Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is \_\_\_\_\_\_\_\_\_\_\_\_. (GATE 2016)   
(A) 100   
(B) 200   
(C) 400   
(D) 500

**Solution:** It can be approached as: 

* The instruction consists of opcode and operands. Given the instruction set of size 12, 4 bits are required for opcode (2^4 = 16).
* As there are total 64 registers, 6 bits are required for identifying a register.
* As the instruction contains 3 registers (2 source + 1 designation), 3 \* 6 = 18 bit are required for register identifiers.
* 12 bits are required for immediate value as given.
* Total bits for an instruction = 4 + 18 + 12 = 34 bits
* The instructions are required to be stored in a byte-aligned fashion. The nearest byte boundary after 34 bits is at 40 bits (5 bytes).
* Hence, for 100 instructions, the memory required is 5 \* 100 = 500 bytes, and the correct option is (D).

A CPU has 12 registers and uses 6 addressing modes.   
RAM is 64K x 32. What is the maximum size of the op-code field if the instruction has a register operand and a memory address operand?

Answer 9 bits.

 